**Features**

• **High-performance, Low-power Atmel**® **AVR**® **8-bit Microcontroller**

• **Advanced RISC Architecture**

**– 131 Powerful Instructions – Most Single-clock Cycle Execution**

**– 32 x 8 General Purpose Working Registers**

**– Fully Static Operation**

**– Up to 16 MIPS Throughput at 16 MHz**

**– On-chip 2-cycle Multiplier**

• **High Endurance Non-volatile Memory segments**

**– 16 Kbytes of In-System Self-programmable Flash program memory**

**– 512 Bytes EEPROM**

**– 1 Kbyte Internal SRAM**

**– Write/Erase Cycles: 10,000 Flash/100,000 EEPROM**

**– Data retention: 20 years at 85°C/100 years at 25°C**(1)

**– Optional Boot Code Section with Independent Lock Bits**

**In-System Programming by On-chip Boot Program**

**True Read-While-Write Operation**

**– Programming Lock for Software Security**

• **JTAG (IEEE std. 1149.1 Compliant) Interface**

**– Boundary-scan Capabilities According to the JTAG Standard**

**– Extensive On-chip Debug Support**

**– Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface**

• **Peripheral Features**

**– Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes**

**– One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture**

**Mode**

**– Real Time Counter with Separate Oscillator**

**– Four PWM Channels**

**– 8-channel, 10-bit ADC**

**8 Single-ended Channels**

**7 Differential Channels in TQFP Package Only**

**2 Differential Channels with Programmable Gain at 1x, 10x, or 200x**

**– Byte-oriented Two-wire Serial Interface**

**– Programmable Serial USART**

**– Master/Slave SPI Serial Interface**

**– Programmable Watchdog Timer with Separate On-chip Oscillator**

**– On-chip Analog Comparator**

• **Special Microcontroller Features**

**– Power-on Reset and Programmable Brown-out Detection**

**– Internal Calibrated RC Oscillator**

**– External and Internal Interrupt Sources**

**– Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby**

**and Extended Standby**

• **I/O and Packages**

**– 32 Programmable I/O Lines**

**– 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF**

• **Operating Voltages**

**– 2.7V - 5.5V for ATmega16L**

**– 4.5V - 5.5V for ATmega16**

• **Speed Grades**

**– 0 - 8 MHz for ATmega16L**

**– 0 - 16 MHz for ATmega16**

• **Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16L**

**– Active: 1.1 mA**

**– Idle Mode: 0.35 mA**

**– Power-down Mode: < 1 μA**

The AVR core combines a rich instruction set with 32 general purpose working registers. All the

32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent

registers to be accessed in one single instruction executed in one clock cycle. The resulting

architecture is more code efficient while achieving throughputs up to ten times faster than conventional

CISC microcontrollers.

The ATmega16 provides the following features: 16 Kbytes of In-System Programmable Flash

Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1 Kbyte SRAM, 32

general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundaryscan,

On-chip Debugging support and programming, three flexible Timer/Counters with compare

modes, Internal and External Interrupts, a serial programmable USART, a byte oriented

Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with

programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator,

an SPI serial port, and six software selectable power saving modes. The Idle mode stops

the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters,

SPI port, and interrupt system to continue functioning. The Power-down mode saves the register

contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt

or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run,

allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC

Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and

ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator

Oscillator is running while the rest of the device is sleeping. This allows very fast start-up

combined with low-power consumption. In Extended Standby mode, both the main Oscillator

and the Asynchronous Timer continue to run.

The device is manufactured using Atmel’s high density nonvolatile memory technology. The Onchip

ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial

interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program

running on the AVR core. The boot program can use any interface to download the application

program in the Application Flash memory. Software in the Boot Flash section will continue to run

while the Application Flash section is updated, providing true Read-While-Write operation. By

combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip,

the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective

solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools

including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators,

and evaluation kits.

**SRAM Data**

**Memory**

Figure 9 shows how the ATmega16 SRAM Memory is organized.

The lower 1120 Data Memory locations address the Register File, the I/O Memory, and the internal

data SRAM. The first 96 locations address the Register File and I/O Memory, and the next

1024 locations address the internal data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement,

Indirect, Indirect with Pre-decrement, and Indirect with Post-increment. In the Register

File, registers R26 to R31 feature the indirect addressing pointer registers.

The direct addressing reaches the entire data space.

The Indirect with Displacement mode reaches 63 address locations from the base address given

by the Y-register or Z-register.

When using register indirect addressing modes with automatic pre-decrement and post-increment,

the address registers X, Y, and Z are decremented or incremented.

The 32 general purpose working registers, 64 I/O Registers, and the 1024 bytes of internal data

SRAM in the ATmega16 are all accessible through all these addressing modes.

**EEPROM Data**

**Memory**

The ATmega16 contains 512 bytes of data EEPROM memory. It is organized as a separate data

space, in which single bytes can be read and written. The EEPROM has an endurance of at

least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described

in the following, specifying the EEPROM Address Registers, the EEPROM Data Register, and

the EEPROM Control Register.

**Table 3.** Number of Watchdog Oscillator Cycles

|  |  |  |
| --- | --- | --- |
| **Typ Time-out (VCC = 5.0V)** | **Typ Time-out (VCC = 3.0V)** | **Number of Cycles** |
| 4.1 ms | 4.3 ms | 4K (4,096) |
| 65 ms | 69 ms | 64K (65,536) |

**Table 17.** Watchdog Timer Prescale Select

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **WDP2** | **WDP1** | **WDP0** | **Number of WDT**  **Oscillator Cycles** | **Typical Time-out**  **at VCC = 3.0V** | **Typical Time-out**  **at VCC = 5.0V** |
| **0** | **0** | **0** | 16K (16,384) | 17.1 ms | 16.3 ms |
| **0** | **0** | **1** | 32K (32,768) | 34.3 ms | 32.5 ms |
| **0** | **1** | **0** | 64K (65,536) | 68.5 ms | 65 ms |
| **0** | **1** | **1** | 128K (131,072) | 0.14 s | 0.13 s |
| **1** | **0** | **0** | 256K (262,144) | 0.27 s | 0.26 s |
| **1** | **0** | **1** | 512K (524,288) | 0.55 s | 0.52 s |
| **1** | **1** | **0** | 1,024K (1,048,576) | 1.1 s | 1.0 s |
| **1** | **1** | **1** | 2,048K (2,097,152) | 2.2 s | 2.1 s |

**8-bit**

**Timer/Counter0**

**with PWM**

Timer/Counter0 is a general purpose, single compare unit, 8-bit Timer/Counter module. The

main features are:

• **Single Compare Unit Counter**

• **Clear Timer on Compare Match (Auto Reload)**

• **Glitch-free, Phase Correct Pulse Width Modulator (PWM)**

• **Frequency Generator**

• **External Event Counter**

• **10-bit Clock Prescaler**

• **Overflow and Compare Match Interrupt Sources (TOV0 and OCF0)**

**16-bit**

**Timer/Counter1**

The 16-bit Timer/Counter unit allows accurate program execution timing (event management),

wave generation, and signal timing measurement. The main features are:

• **True 16-bit Design (that is, allows 16-bit PWM)**

• **Two Independent Output Compare Units**

• **Double Buffered Output Compare Registers**

• **One Input Capture Unit**

• **Input Capture Noise Canceler**

• **Clear Timer on Compare Match (Auto Reload)**

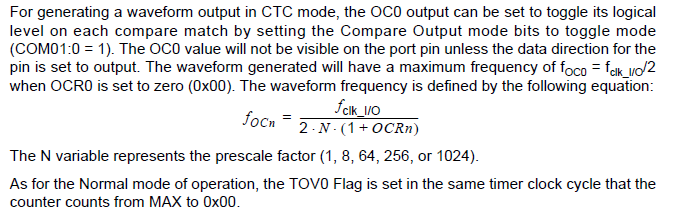
• **Glitch-free, Phase Correct Pulse Width Modulator (PWM)**

• **Variable PWM Period**

• **Frequency Generator**

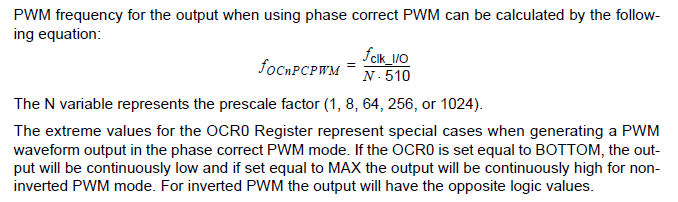
• **External Event Counter**

• **Four Independent Interrupt Sources (TOV1, OCF1A, OCF1B, and ICF1)**



**Table 42.** Clock Select Bit Description Timer/Counter 0/1

|  |  |  |  |
| --- | --- | --- | --- |
| **CS02/12** | **CS01/11** | **CS00/10** | **Description** |
| 0 | 0 | 0 | No clock source (Timer/Counter stopped). |
| 0 | 0 | 1 | clkI/O/(No prescaling) |
| 0 | 1 | 0 | clkI/O/8 (From prescaler) |
| 0 | 1 | 1 | clkI/O/64 (From prescaler) |
| 1 | 0 | 0 | clkI/O/256 (From prescaler) |
| 1 | 0 | 1 | clkI/O/1024 (From prescaler) |
| 1 | 1 | 0 | External clock source on T0/T1 pin. Clock on falling edge. |
| 1 | 1 | 1 | External clock source on T0/T1 pin. Clock on rising edge. |

****

**8-bit Timer/Counter2 with PWM and Asynchronous Operation**

Timer/Counter2 is a general purpose, single compare unit, 8-bit Timer/Counter module. The

main features are:

• **Single Compare unit Counter**

• **Clear Timer on Compare Match (Auto Reload)**

• **Glitch-free, Phase Correct Pulse Width Modulator (PWM)**

• **Frequency Generator**

• **10-bit Clock Prescaler**

• **Overflow and Compare Match Interrupt Sources (TOV2 and OCF2)**

• **Allows clocking from External 32 kHz Watch Crystal Independent of the I/O Clock**

**Table 54.** Clock Select Bit Description Timer/Counter2

|  |  |  |  |
| --- | --- | --- | --- |
| **CS22** | **CS21** | **CS20** | **Description** |
| 0 | 0 | 0 | No clock source (Timer/Counter stopped). |
| 0 | 0 | 1 | clkI/O/(No prescaling) |
| 0 | 1 | 0 | clkI/O/8 (From prescaler) |
| 0 | 1 | 1 | clkI/O/32 (From prescaler) |
| 1 | 0 | 0 | clkI/O/64 (From prescaler) |
| 1 | 0 | 1 | clkI/O/128 (From prescaler) |
| 1 | 1 | 0 | clkI/O/256 (From prescaler) |
| 1 | 1 | 1 | clkI/O/1024 (From prescaler). |

**USART**

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a

highly flexible serial communication device. The main features are:

• Full Duplex Operation (Independent Serial Receive and Transmit Registers)

• Asynchronous or Synchronous Operation

• Master or Slave Clocked Synchronous Operation

• High Resolution Baud Rate Generator

• Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits

• Odd or Even Parity Generation and Parity Check Supported by Hardware

• Data OverRun Detection

• Framing Error Detection

• Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter

• Three Separate Interrupts on TX Complete, TX Data Register Empty, and RX Complete

• Multi-processor Communication Mode

• Double Speed Asynchronous Communication Mode

**Table 60. Equations for Calculating Baud Rate Register Setting**

|  |  |  |
| --- | --- | --- |
| **Operating Mode** | **Equation for Calculating**  **Baud Rate**(1) | **Equation for**  **Calculating UBRR**  **Value** |
| Asynchronous Normal Mode(U2X = 0) | BAUD= | *UBBR=* |
| Asynchronous Double Speed Mode (U2X = 1) | *BAUD=* | *UBBR=* |
| Synchronous Master Mode | *BAUD=* | *UBBR=* |

Note: 1. The baud rate is defined to be the transfer rate in bit per second (bps).

BAUD Baud rate (in bits per second, bps)

fOSC System Oscillator clock frequency

UBRR Contents of the UBRRH and UBRRL Registers, (0 - 4095)

Error[%]*=*

**Asynchronous Operational Range**

The operational range of the receiver is dependent on the mismatch between the received bit

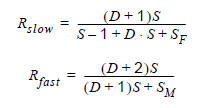
rate and the internally generated baud rate. If the Transmitter is sending frames at too fast or too

slow bit rates, or the internally generated baud rate of the receiver does not have a similar

base frequency, the receiver will not be able to synchronize the frames to the start bit.

The following equations can be used to calculate the ratio of the incoming data rate and internal

receiver baud rate.



D Sum of character size and parity size (D = 5 to 10 bit)

S Samples per bit. S = 16 for Normal Speed mode and S = 8 for

Double Speed mode.

SF First sample number used for majority voting. SF = 8 for Normal Speed and

SF = 4 for Double Speed mode.

SM Middle sample number used for majority voting. SM = 9 for Normal Speed and

SM = 5 for Double Speed mode.

Rslow is the ratio of the slowest incoming data rate that can be accepted in relation to the

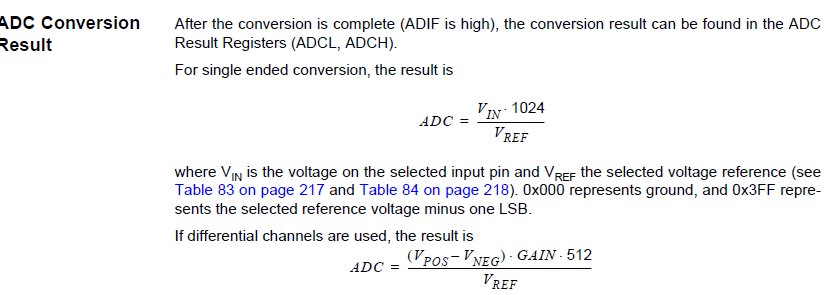
receiver baud rate. Rfast is the ratio of the fastest incoming data rate that can be

accepted in relation to the receiver baud rate.

**Table 81. ADC Conversion Time**

|  |  |  |
| --- | --- | --- |
| **Condition** | **Sample & Hold (Cycles from Start of Conversion)** | **Conversion Time (Cycles)** |
| First conversion | 13.5 | 25 |
| Normal conversions, single ended | 1.5 | 13 |
| Auto Triggered conversions | 2 | 13.5 |
| Normal conversions, differential | 1.5/2.5 | 13/14 |

**ADC**

****

**Table 85.** ADC Prescaler Selections

|  |  |  |  |
| --- | --- | --- | --- |
| **ADPS2** | **ADPS1** | **ADPS0** | **Division factor** |
| 0 | 0 | 0 | 2 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 32 |
| 1 | 1 | 0 | 64 |
| 1 | 1 | 1 | 128 |

**JTAG Interface and On-chip Debug System**

**Features**

• **JTAG (IEEE std. 1149.1 Compliant) Interface**

• **Boundary-scan Capabilities According to the IEEE std. 1149.1 (JTAG) Standard**

• **Debugger Access to:**

**– All Internal Peripheral Units**

**– Internal and External RAM**

**– The Internal Register File**

**– Program Counter**

**– EEPROM and Flash Memories**

**– Extensive On-chip Debug Support for Break Conditions, Including**

**– AVR *Break* Instruction**

**– Break on Change of Program Memory Flow**

**– Single Step Break**

**– Program Memory Breakpoints on Single Address or Address Range**

**– Data Memory Breakpoints on Single Address or Address Range**

• **Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface**

**Electrical Characteristics**

**Absolute Maximum Ratings\***

Operating Temperature.................................. -55°C to +125°C \*NOTICE: Stresses beyond those listed under “Absolute

Maximum Ratings” may cause permanent damage

to the device. This is a stress rating only and

functional operation of the device at these or

other conditions beyond those indicated in the

operational sections of this specification is not

implied. Exposure to absolute maximum rating

conditions for extended periods may affect

device reliability.

Storage Temperature ..................................... -65°C to +150°C

Voltage on any Pin except RESET

with respect to Ground ................................-0.5V to VCC+0.5V

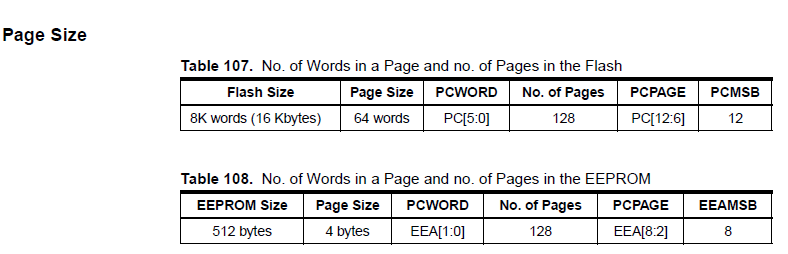
Voltage on RESET with respect to Ground......-0.5V to +13.0V

Maximum Operating Voltage ............................................ 6.0V

DC Current per I/O Pin ............................................... 40.0 mA

DC Current VCC and GND Pins................ 200.0 mA PDIP and

400.0 mA TQFP/MLF



**Table 119.** External RC Oscillator, Typical Frequencies (VCC = 5)

|  |  |  |
| --- | --- | --- |
| **R [k**Ω**]**(1) | **C [pF]** | **f**(2) |
| 33 | 22 | 650 kHz |
| 10 | 22 | 2.0 MHz |

